

Amendments to the Claims

Claims 1 to 26 (Cancelled)

27. (New) A processing core of a processing system for processing information, comprising:

a processing unit;

an instruction cache and a code random access memory coupled to the processing unit;

a register group and another register group coupled to the processing unit;

a data memory and another data memory coupled to the processing unit; and

a low priority interrupt controller and a high priority interrupt controller coupled to the processing unit; and

wherein the instruction cache, the register group, the data memory, and the low priority interrupt controller are dedicated to performing non-time-critical tasks by the processing unit; and

wherein the code random access memory, the another register group, the another data memory, and the high priority interrupt controller are dedicated to performing time-critical tasks by the processing unit.

28. (New) The processing core according to Claim 27, wherein one of the time-critical tasks is providing additional data to a video engine unit during a video compression process.

29. (New) The processing core according to Claim 28, wherein the additional data is provided to the video engine unit within a time interval of less than two microseconds.
30. (New) The processing core according to Claim 27, wherein one of the non-time-critical tasks is multiplexing of audio and video streams.
31. (New) The processing core according to Claim 27, wherein one of the non-time-critical tasks is demultiplexing Motion Picture Expert Group (MPEG) streams.
32. (New) The processing core according to Claim 27, wherein the non-time-critical tasks are user interface applications.
33. (New) The processing core according to Claim 32, wherein one of the user interface applications is providing an on-screen display every two seconds.
34. (New) A method of processing information by a processing core for a processing system, comprising:
- providing a processing unit;
 - coupling an instruction cache and a code random access memory to the processing unit;
 - coupling a register group and another register group to the processing unit;
 - coupling a data memory and another data memory to the processing unit;

coupling a low priority interrupt controller and a high priority interrupt controller to the processing unit;

performing non-time-critical tasks through dedicated use by the processing unit of the instruction cache, the register group, the data memory, and the low priority interrupt controller; and

performing time-critical tasks through dedicated use by the processing unit of the code random access memory, the another register group, the another data memory, and the high priority interrupt controller.

35. (New) The method according to Claim 34, wherein performing time-critical tasks further comprises providing additional data to a video engine unit during a video compression process.

36. (New) The method according to Claim 35, wherein providing additional data further comprises providing the additional data to the video engine unit within a time interval of less than two microseconds.

37. (New) The method according to Claim 34, wherein performing non-time-critical tasks further comprises multiplexing of audio and video streams.

38. (New) The method according to Claim 34, wherein performing non-time-critical tasks further comprises demultiplexing Motion Picture Expert Group (MPEG) streams.

39. (New) The method according to Claim 34, wherein performing non-time-critical tasks further comprises performing user interface applications.
40. (New) The method according to Claim 39, wherein performing user interface applications further comprises providing an on-screen display every two seconds.
41. (New) An audio and video encoder/decoder, comprising:
- a processing system;
 - a video engine unit and a video interface unit both coupled to the processing system;
 - an audio engine unit and an audio interface unit both coupled to the processing system; and
- wherein the processing system has a processing core that includes:
- a processing unit;
 - an instruction cache and a code random access memory coupled to the processing unit;
 - a register group and another register group coupled to the processing unit;
 - a data memory and another data memory coupled to the processing unit;
- and
- a low priority interrupt controller and a high priority interrupt controller coupled to the processing unit; and

wherein the instruction cache, the register group, the data memory, and the low priority interrupt controller are dedicated to performing non-time-critical tasks by the processing unit; and

wherein the code random access memory, the another register group, the another data memory, and the high priority interrupt controller are dedicated to performing time-critical tasks by the processing unit.

42. (New) The audio and video encoder/decoder according to Claim 41, wherein one of the time-critical tasks is providing additional data to a video engine unit during a video compression process.

43. (New) The audio and video encoder/decoder according to Claim 42, wherein the additional data is provided to the video engine unit within a time interval of less than two microseconds.

44. (New) The audio and video encoder/decoder according to Claim 41, wherein one of the non-time-critical tasks is multiplexing of audio and video streams.

45. (New) The audio and video encoder/decoder according to Claim 41, wherein one of the non-time-critical tasks is demultiplexing Motion Picture Expert Group (MPEG) streams.

46. (New) The audio and video encoder/decoder according to Claim 41, wherein the non-time-critical tasks are user interface applications.

47. (New) The audio and video encoder/decoder according to Claim 46, wherein one of the user interface applications is providing an on-screen display every two seconds.